



RS780M-A2

V : A

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REVISION HISTORY:

Rev	Date	Notes
VA	2008/08/12	

Modify RS780D

DEL	ADD
1. SP	1. JMB361(ESATA)
2. PCIE SW	2. +1 PCI
3. -1 PCIE x16	3. POWER LED
4. -1 LAN 8112	
5. 1394	
6. 4PIN POWER	

PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTON

IMPORTANT NOTES ABOUT THIS SCHEMATIC

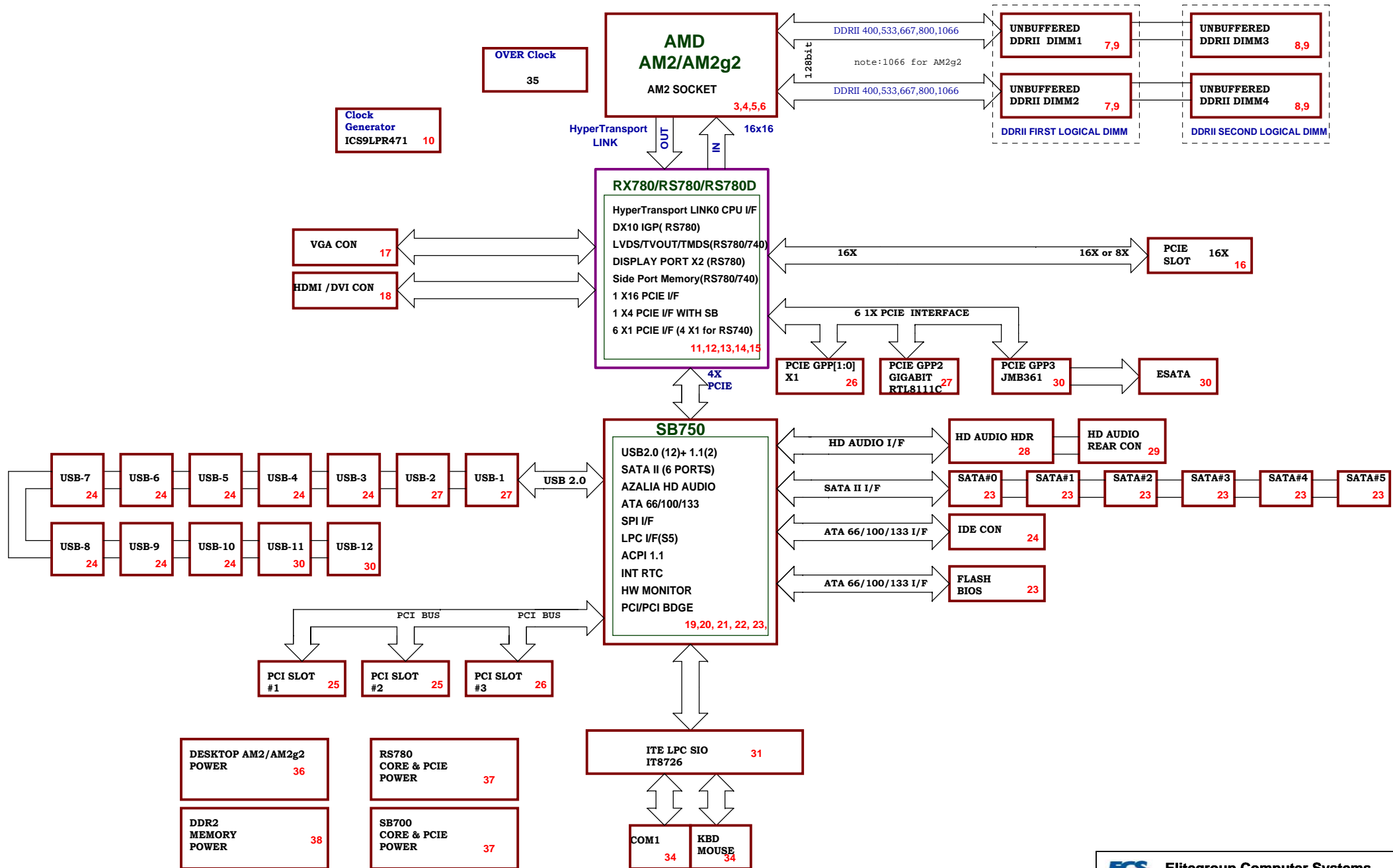
DESIGN NOTE: Example text for the design note to show the note inside the colored box.

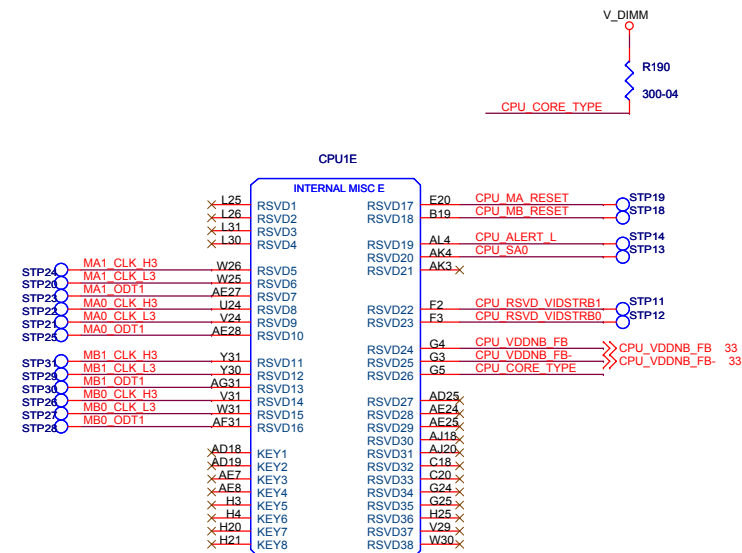
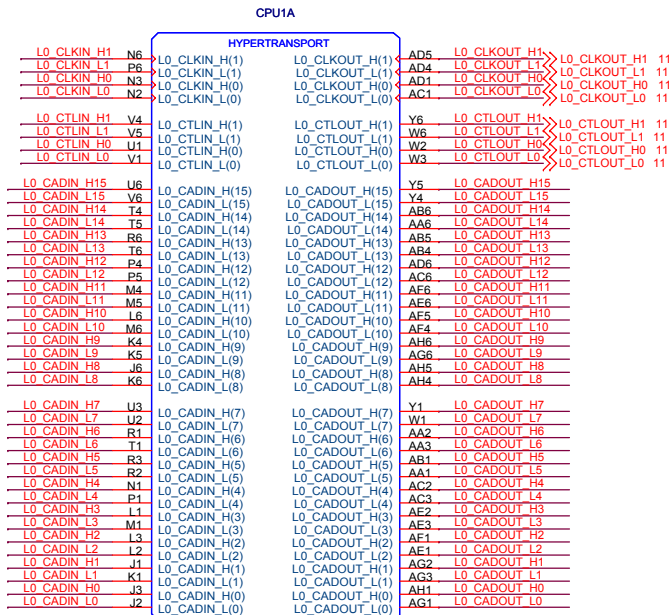
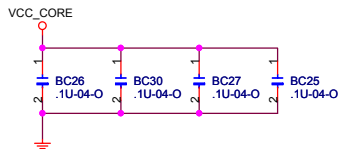
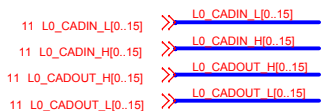
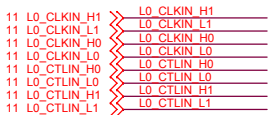
1) DESIGN NOTES in grey are information notes.

DESIGN NOTE: Example text for the design note to show the note inside the colored box.

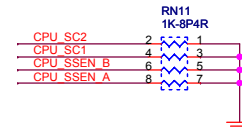
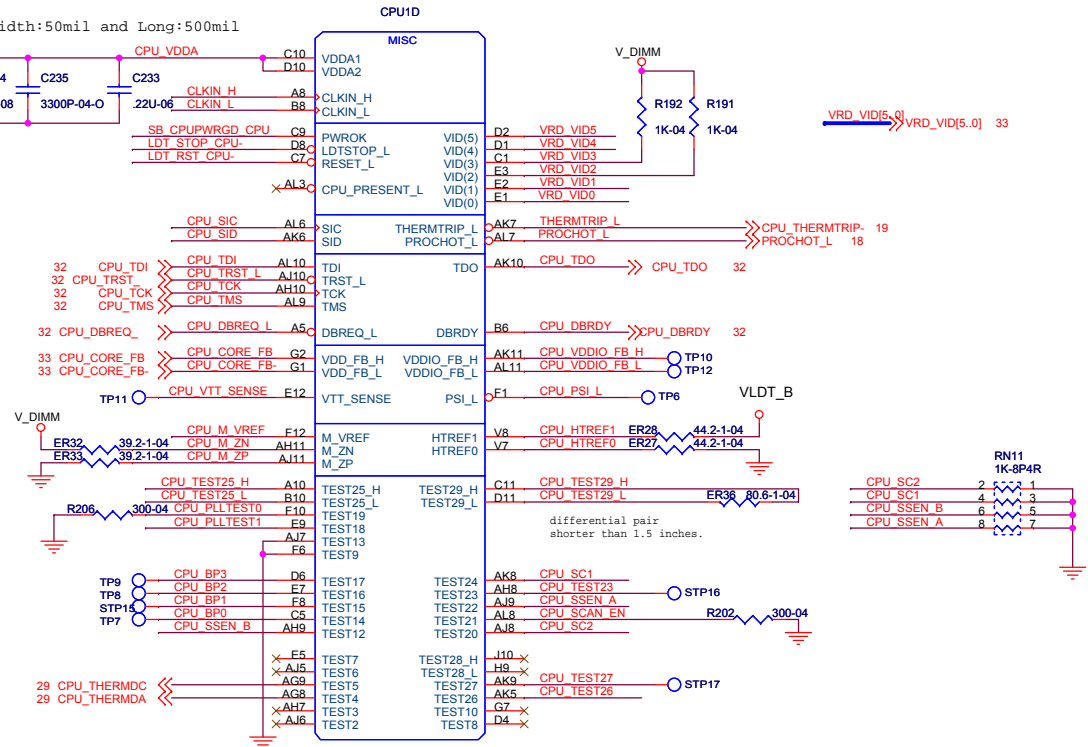
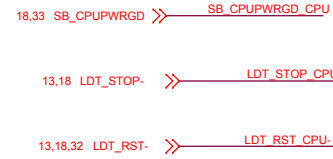
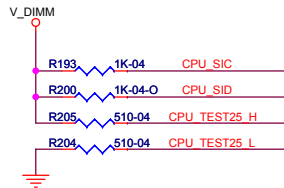
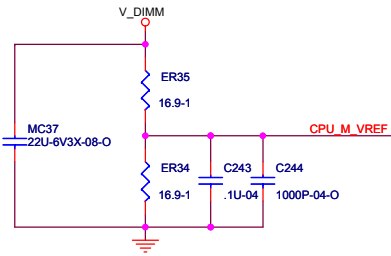
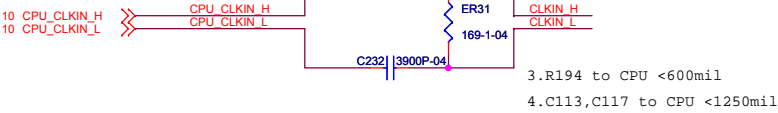
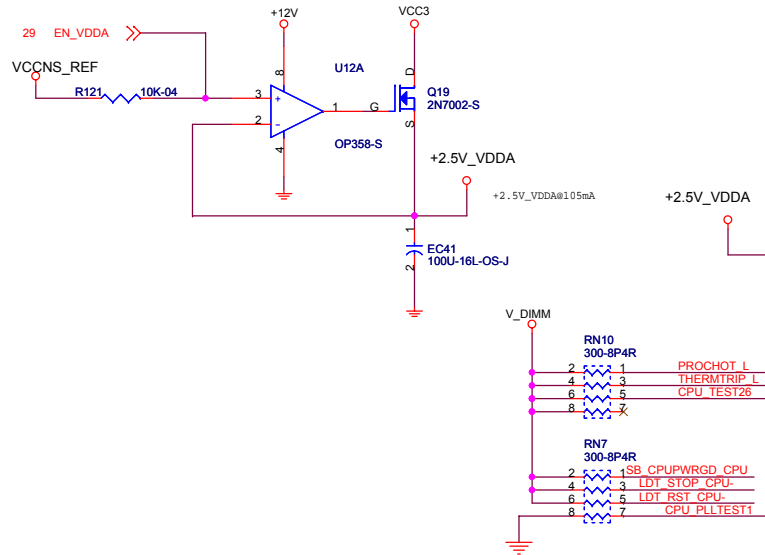
2) DESIGN NOTES in yellow are notes of caution.

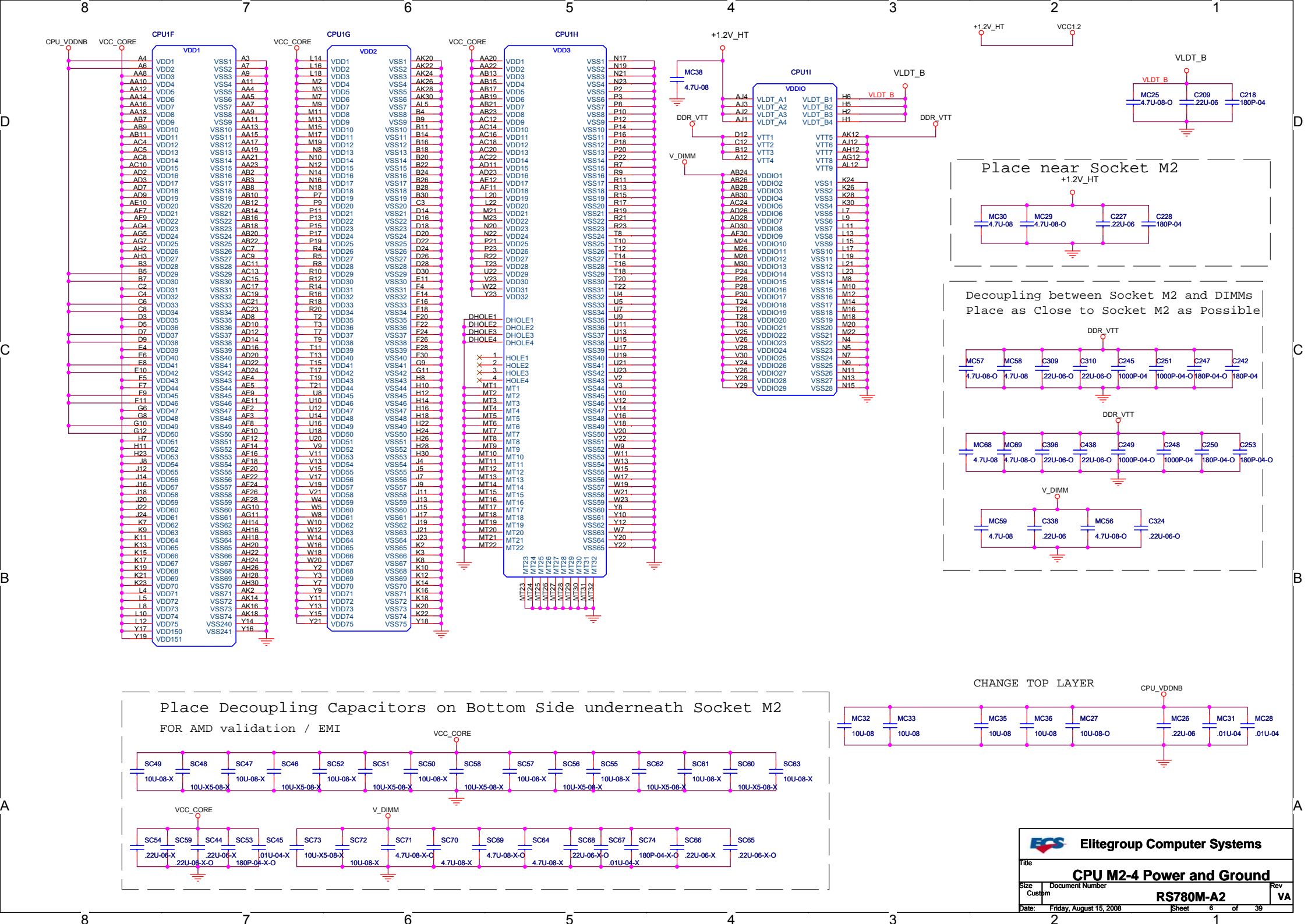
3) DESIGN NOTES in red are critical, and must be understood and followed.

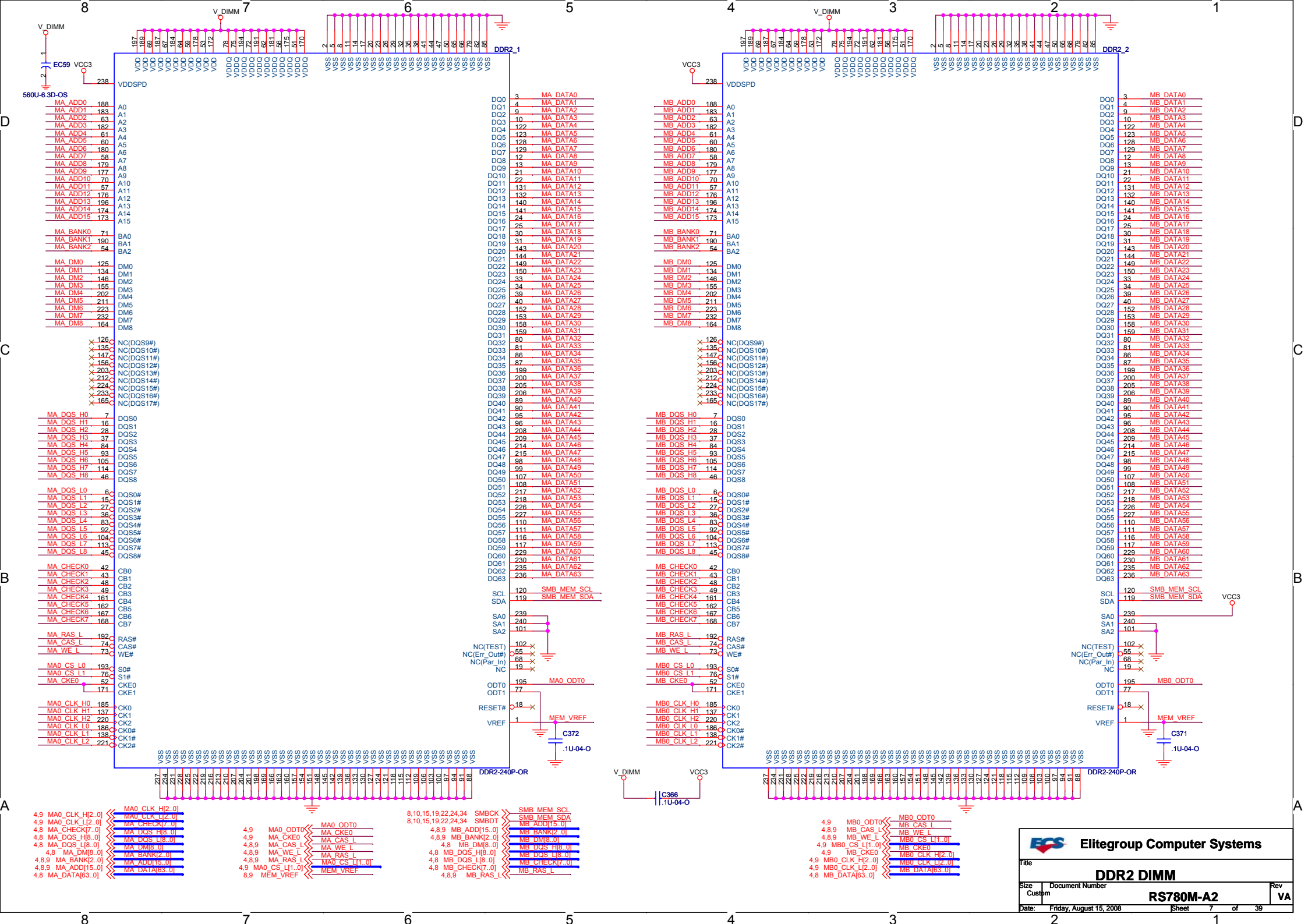


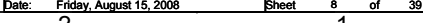


+2.5V_VDDA for CPU PLL











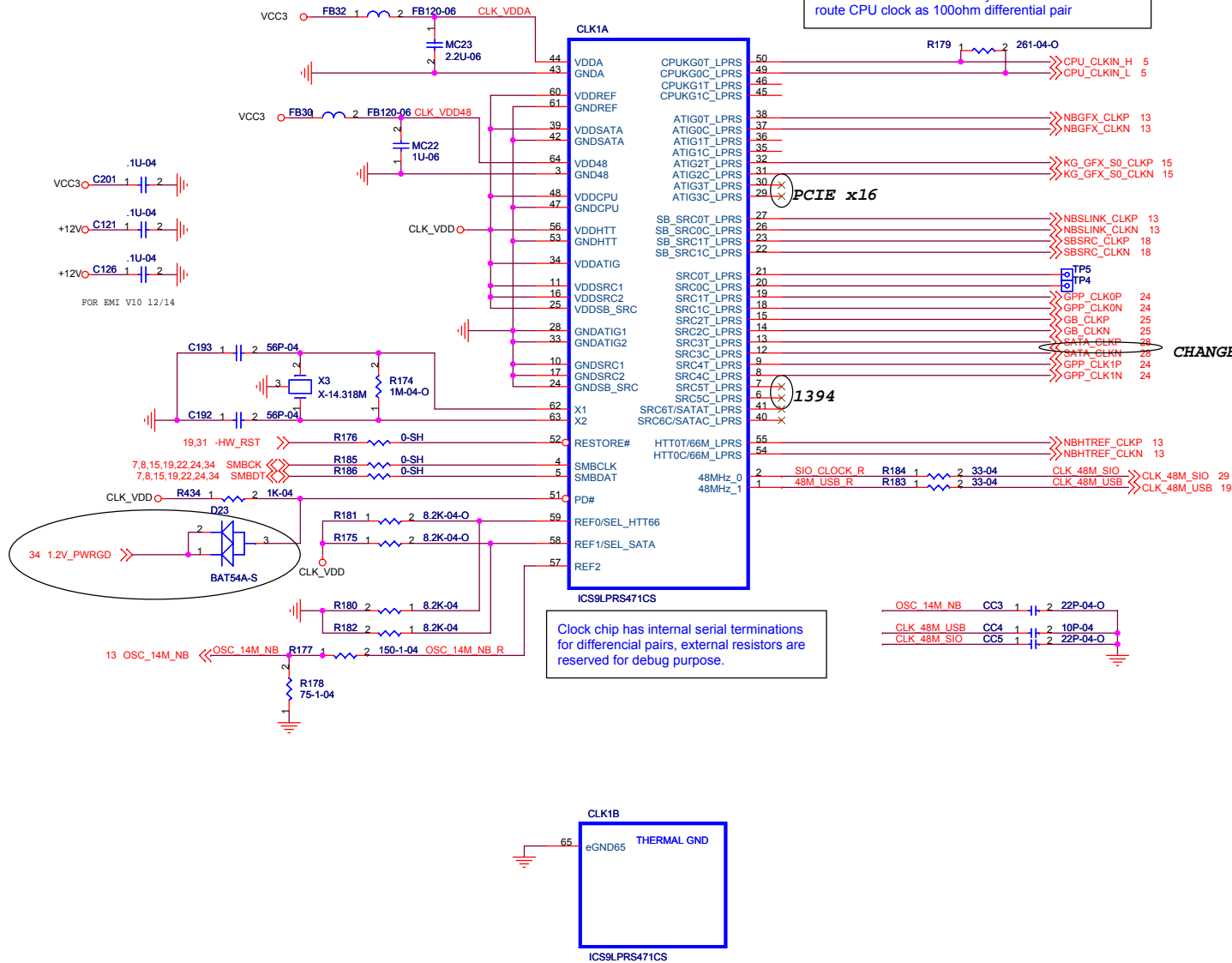
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.

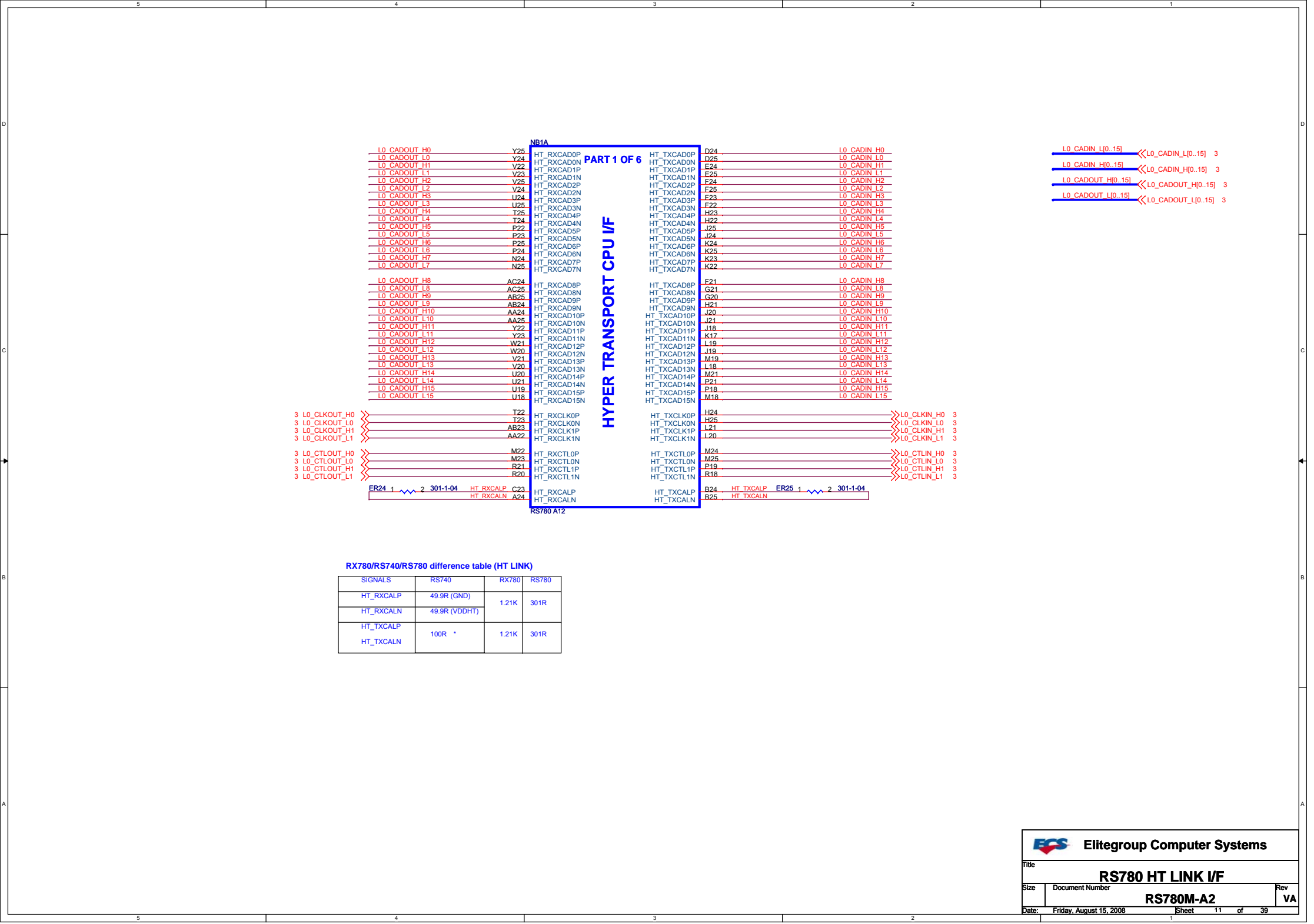


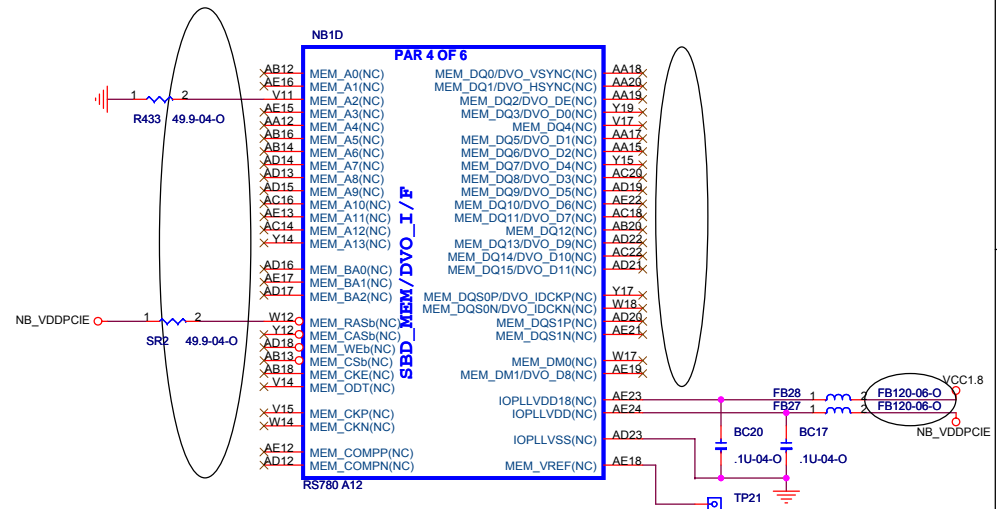
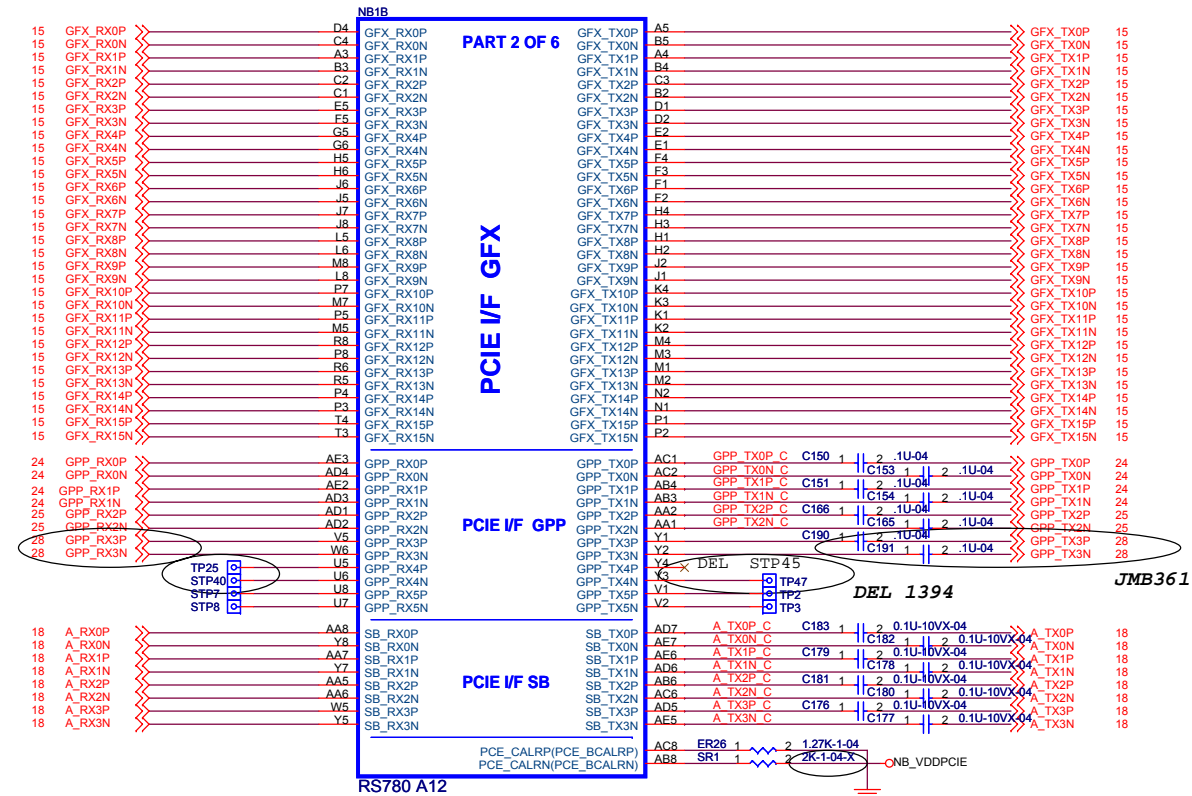
CHANGE TO JMB361

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 75R/100R
RS780 (Single-ended)	1.1V 150R/75R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK





RS780 GFX Slot Routing table

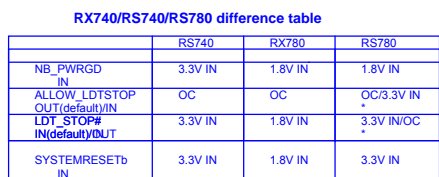
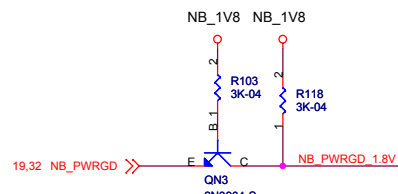
GFX_MODE_SELECT	GFX SLOTS MODE
0	X16 LANES MODE (DEFAULT)
1	TWO X8 LANES MODE

RS780 GPP Routing table

GPP X4 CONNECTOR	GPP[3:0]
GPP X1 CONNECTOR	GPP4
SIGABIT ETHERNET	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3
	AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7
	AUX1 and HPD1

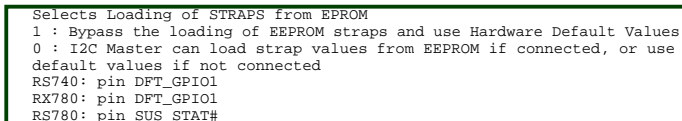
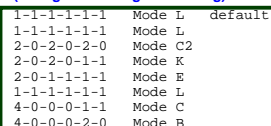
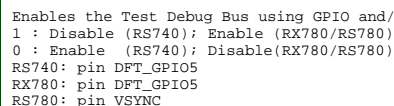


The image displays three circuit diagrams for connecting the L9640 module to an external microcontroller.

Top Diagram (LDT_STOP): Shows the connection of the LDT_STOP pin (pin 5, 18) to the L9640 module. The pin is connected to the E (emitter) of a 2N3904-S transistor (QN4). The base of the transistor is connected to VCC1.8 through a 4.7K-04 resistor (R107). The collector of the transistor is connected to VCC3 through a 4.7K-04 resistor (R111). The L9640 module pin is connected to the collector of the transistor and is labeled LDSTOP.

Middle Diagram (LDT_RST): Shows the connection of the LDT_RST pin (pins 5, 18, 32) to the L9640 module. The pin is connected to the E (emitter) of a 2N3904-S transistor (QN2). The base of the transistor is connected to VCC1.8 through a 4.7K-04 resistor (R102). The collector of the transistor is connected to VCC3 through a 4.7K-04 resistor (R117). The L9640 module pin is connected to the collector of the transistor and is labeled NB_RST_1.8V.

Bottom Diagram (NB output): Shows the connection of the NB output pin to the L9640 module. The pin is connected to the L9640 module pin and is labeled NB output is OD pin. The pin is also connected to VCC1.8 through a 1K-04 resistor (R129). The L9640 module pin is labeled ALLOW_LDTSTOP_NB.

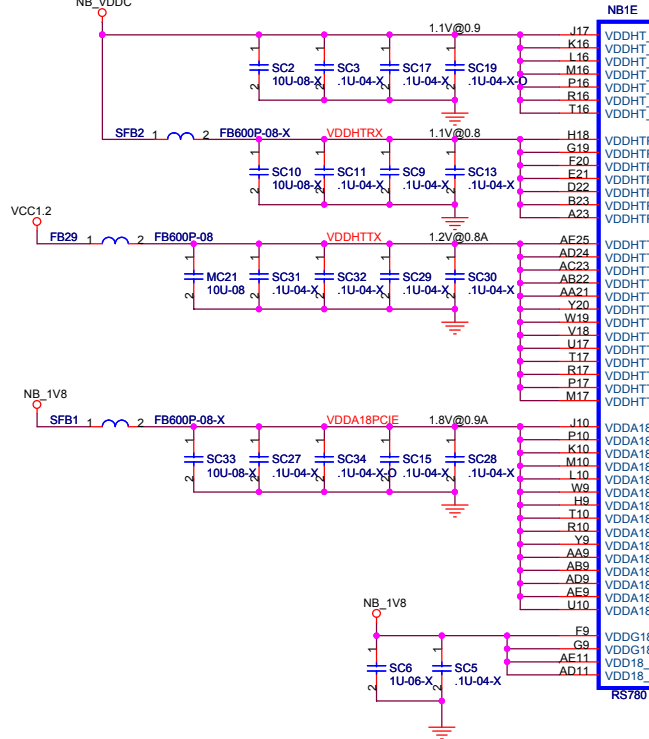


NB1F
RS780 A12

PART 6/6

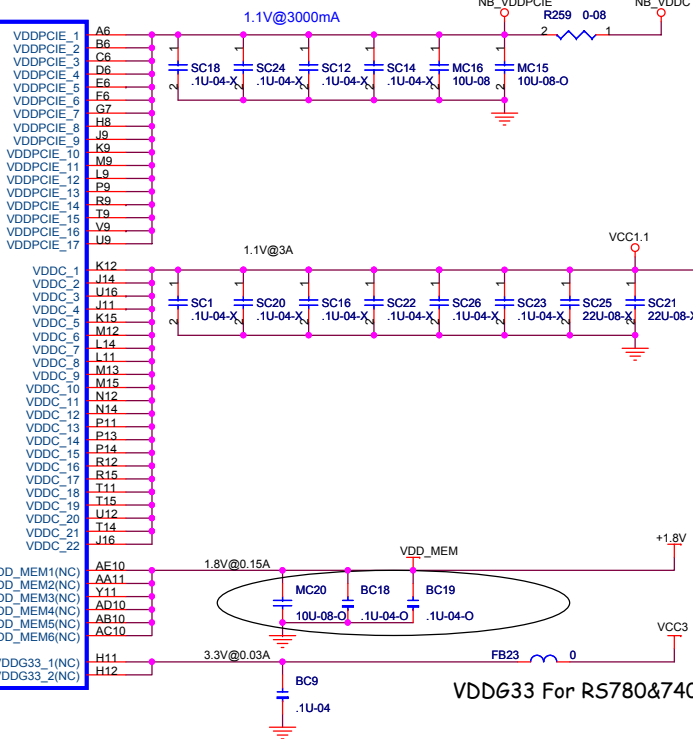
GROUND

Please use 1mm pad size,
place all ELT test pads
on bottom side only

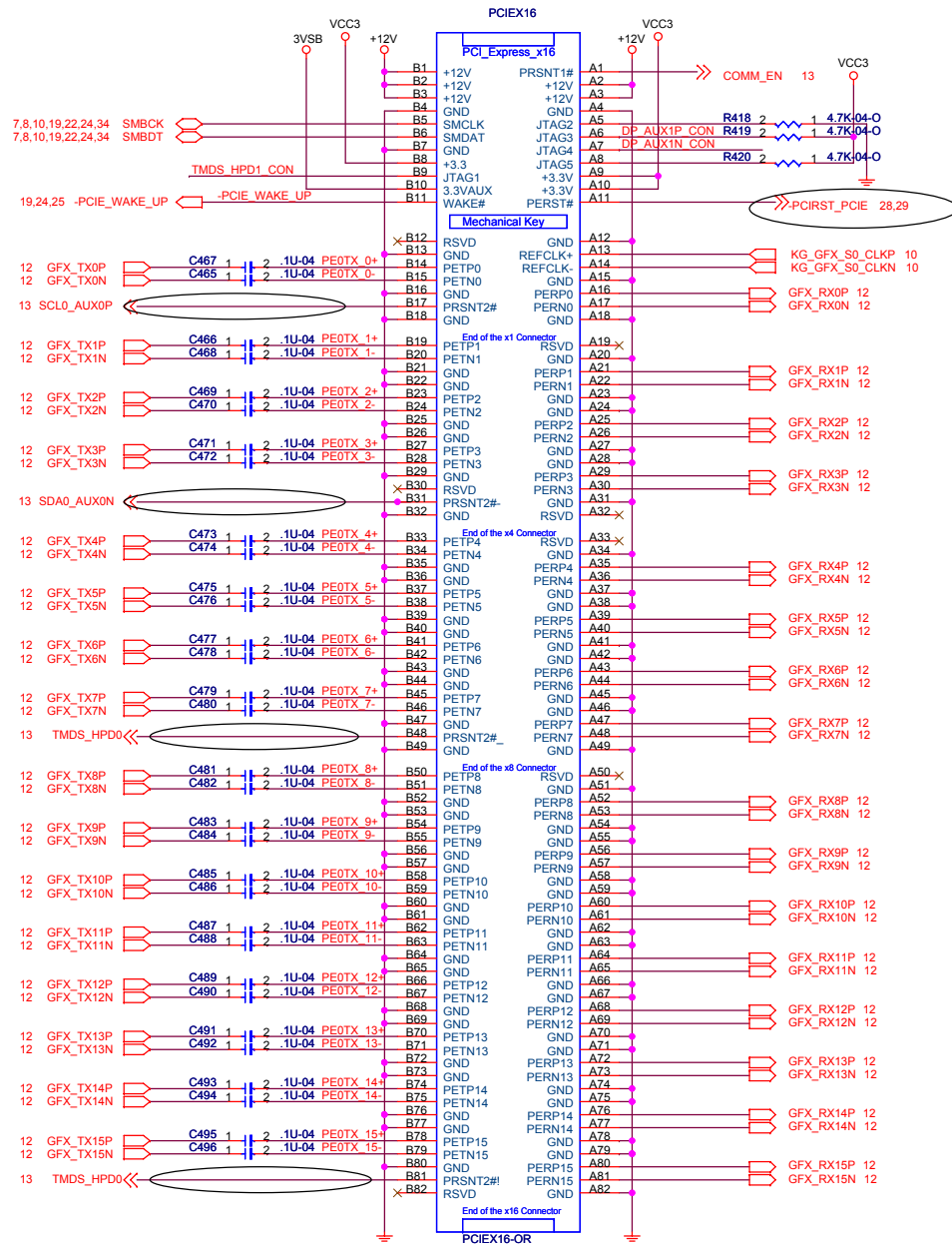


PART 5/6

POWER

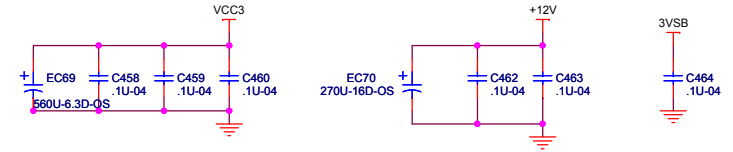


VDDG33 For RS780&740

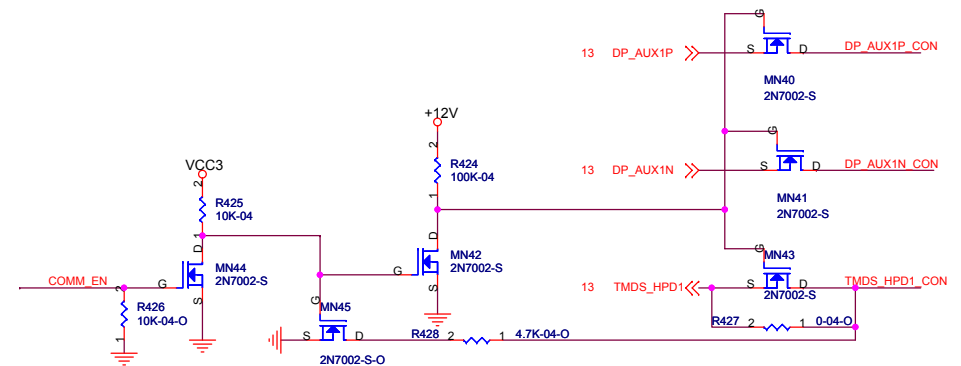


DEL PCIe x16

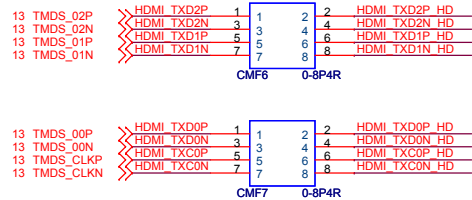
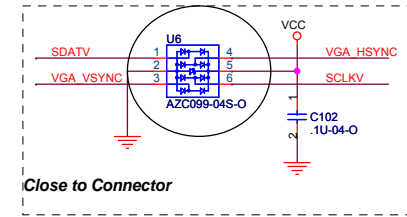
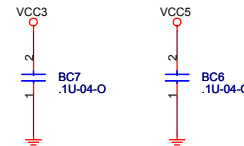
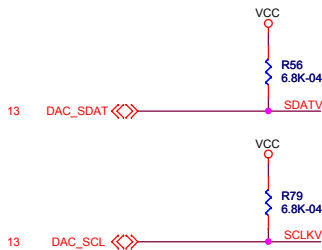
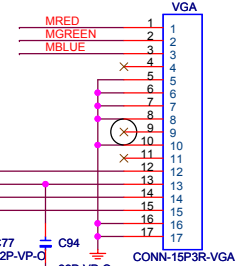
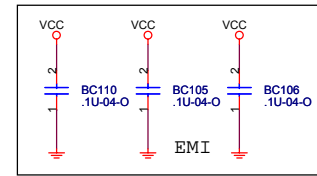
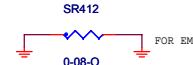
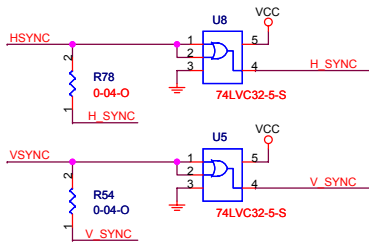
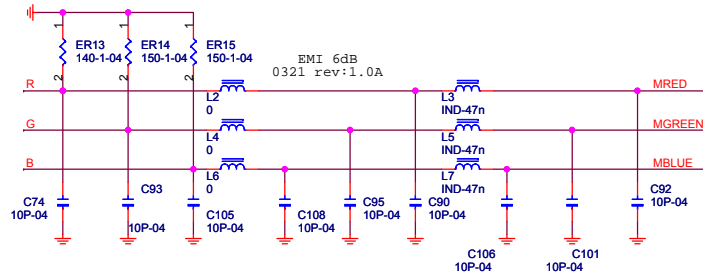
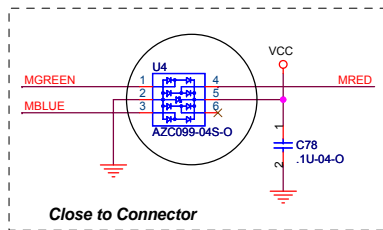
DEL 4PinPower



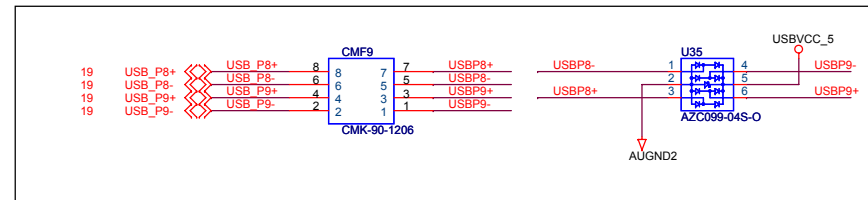
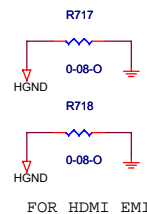
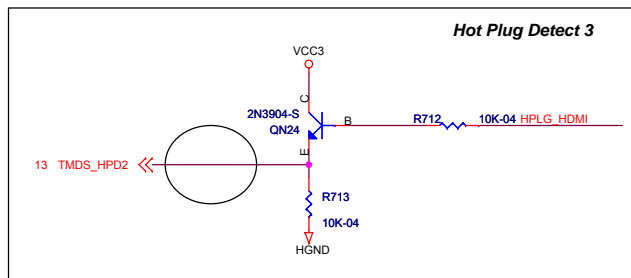
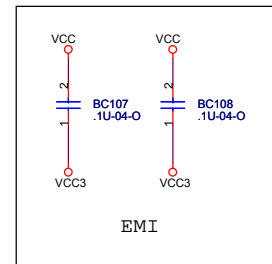
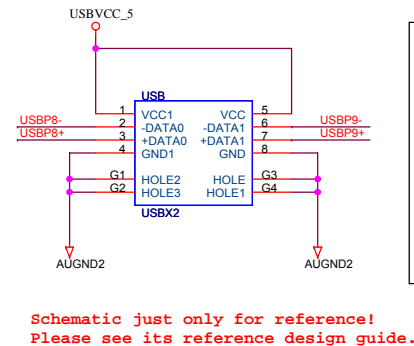
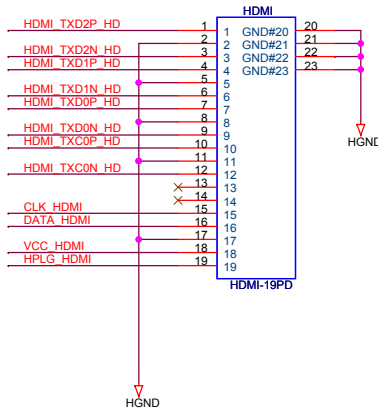
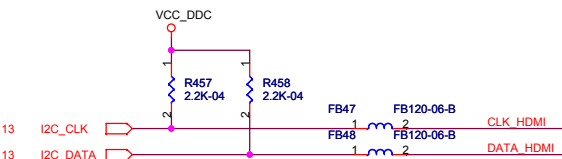
SWITCH CIRCUIT FOR SECONDARY DISPLAYPORT



External Connection



VCC_DDC





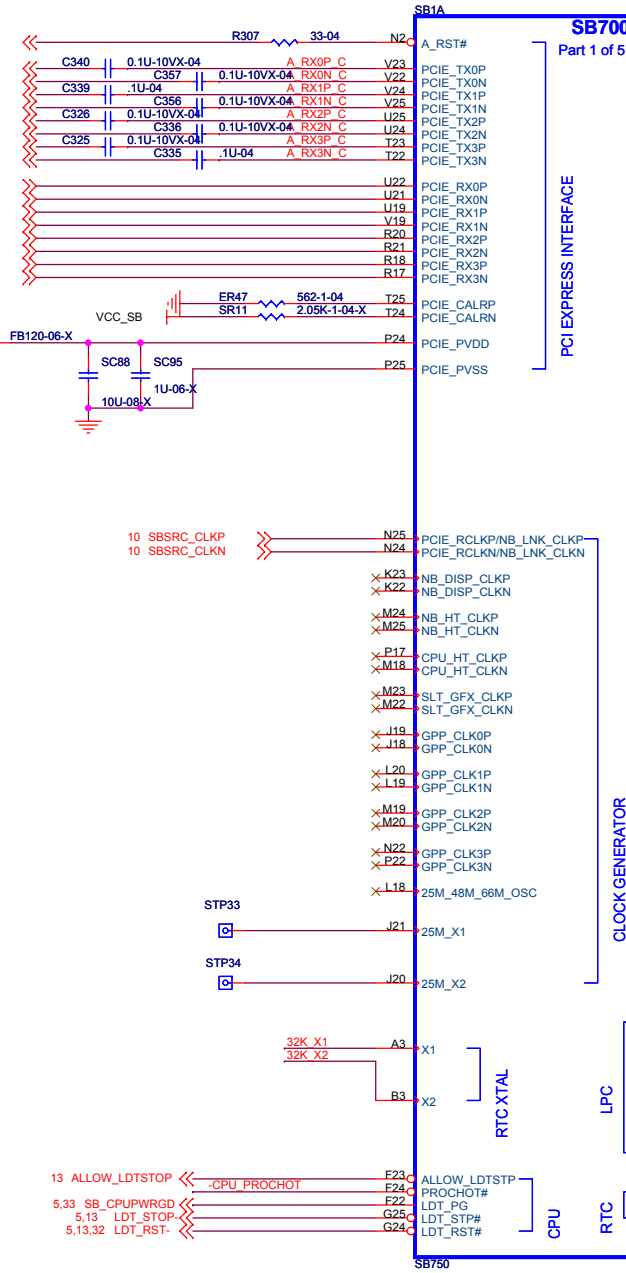
SB700A11



PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB700

- 13.29 -A_RST
12 A_RX0P
12 A_RX0N
12 A_RX1P
12 A_RX1N
12 A_RX2P
12 A_RX2N
12 A_RX3P
12 A_RX3N

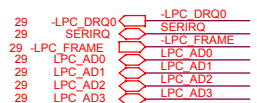
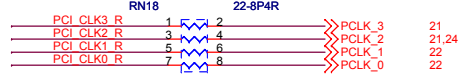
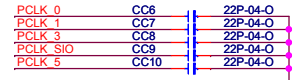
12 A_TX0P
12 A_TX0N
12 A_TX1P
12 A_TX1N
12 A_TX2P
12 A_TX2N
12 A_TX3P
12 A_TX3N



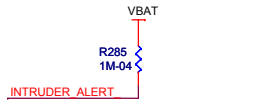
POWER EXPRESS SUPPORT

PE_GPIO0 MXM RESET	H: Enable
PE_GPIO1 MXM POWER ENABLE	H: Enable
PE_GPIO2 MODE SWITCH	H:MXM L:NB
TMDS_HPD0 MXM HOT PLUG	

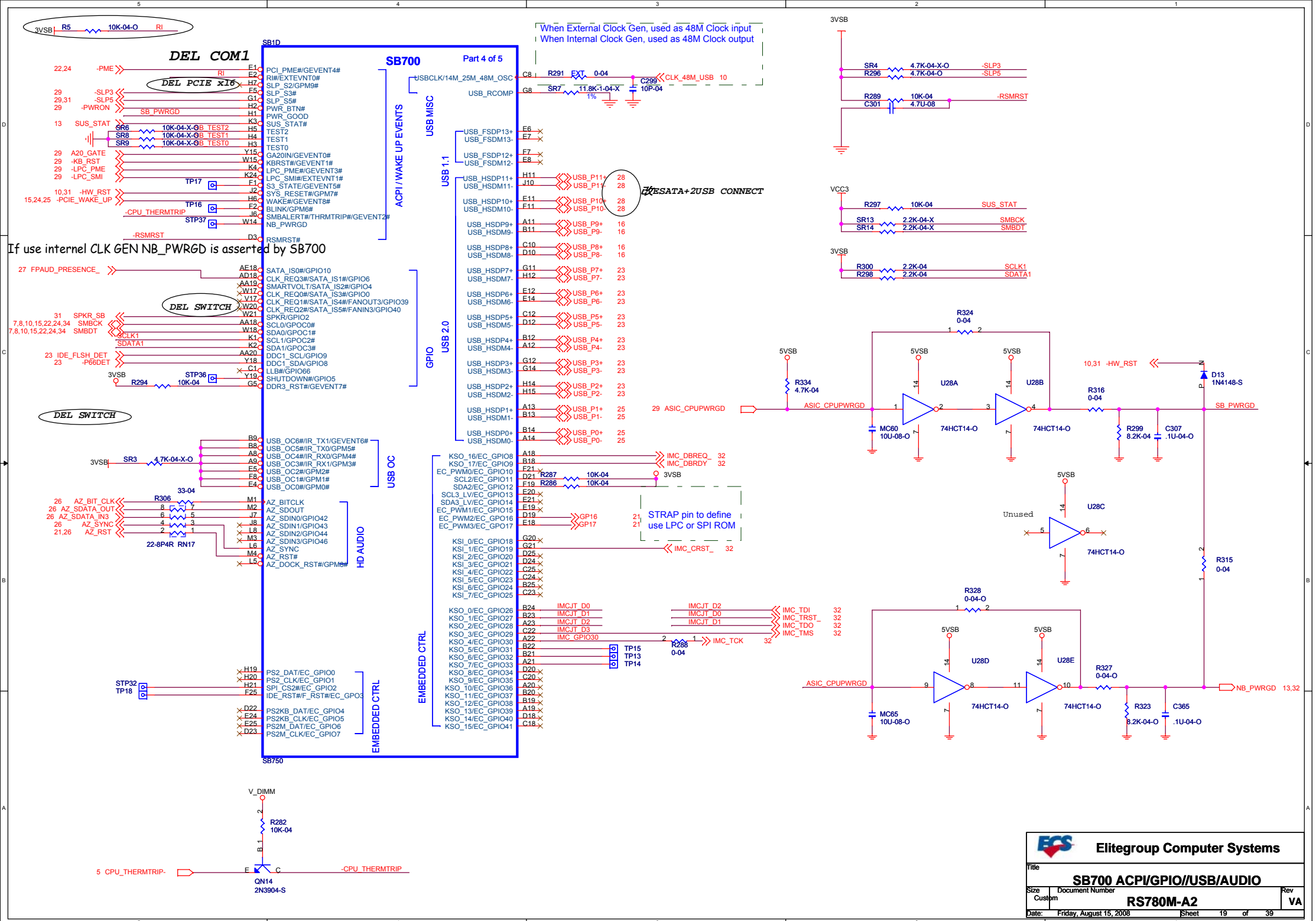
PCLK_2/3/5 not need match length because use as SB700 Stamps only.



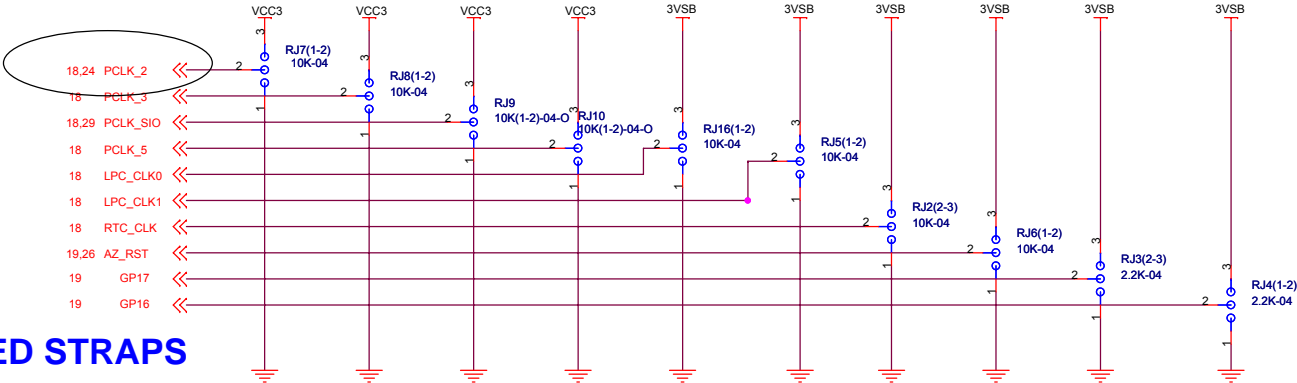
For PCI3



1-2: NORMAL
2-3: CMOS CLEAR



NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



REQUIRED STRAPS

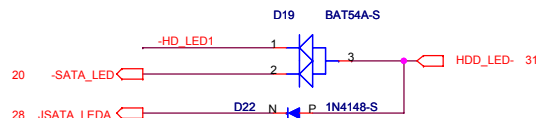
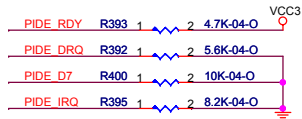
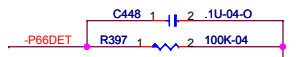
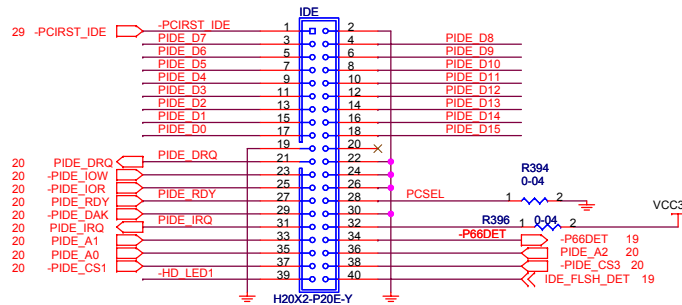
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			IMC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM	

DEBUG STRAPS SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

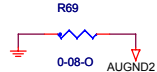
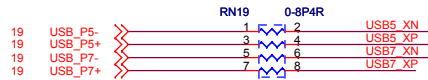
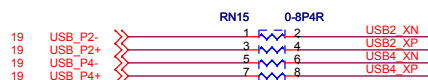
Del PCIE Debug EEPROM Strap

Del Debug straps 070423

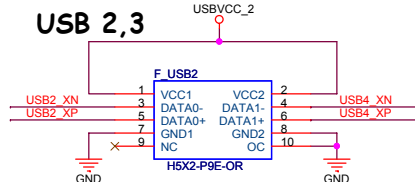
20 PIDE_D[15:0]



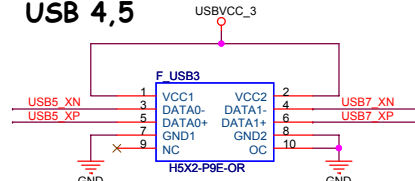
change to bat54a for space 6/8



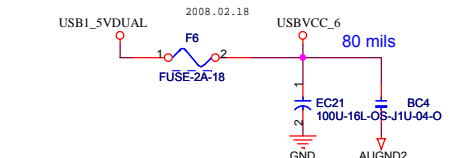
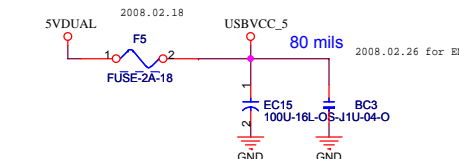
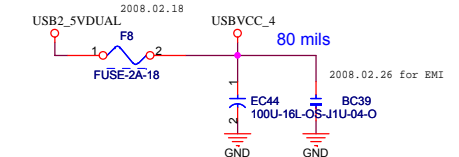
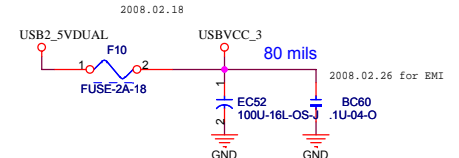
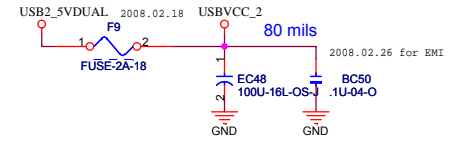
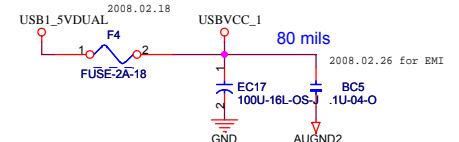
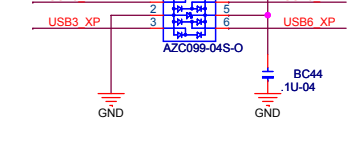
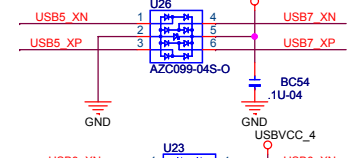
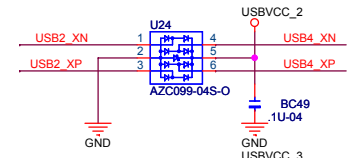
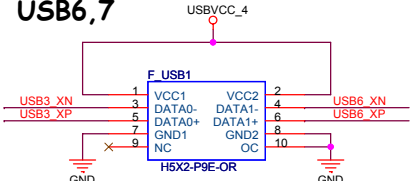
USB 2,3



USB 4,5



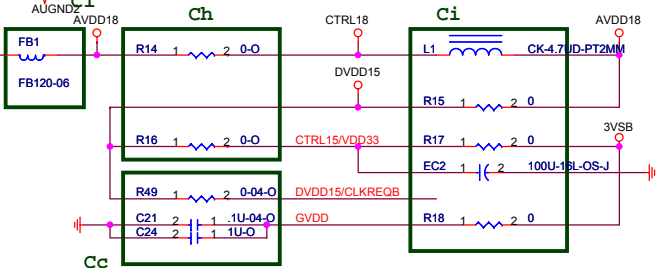
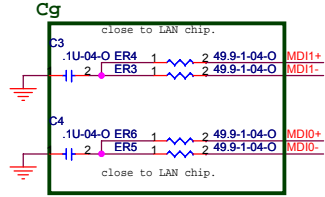
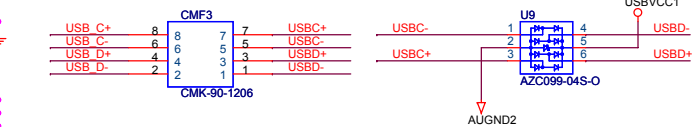
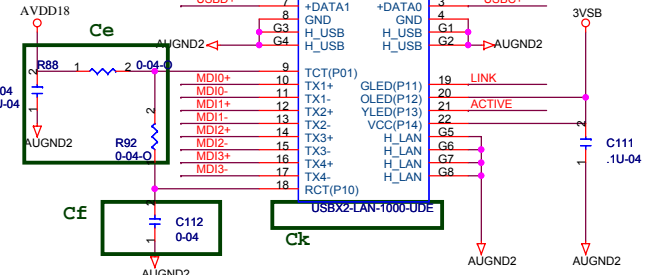
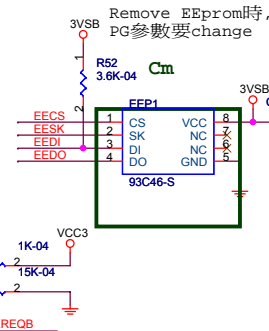
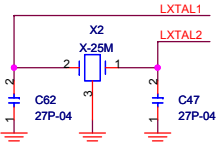
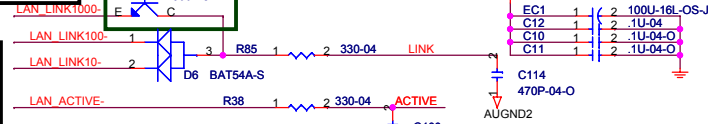
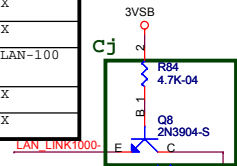
USB6,7

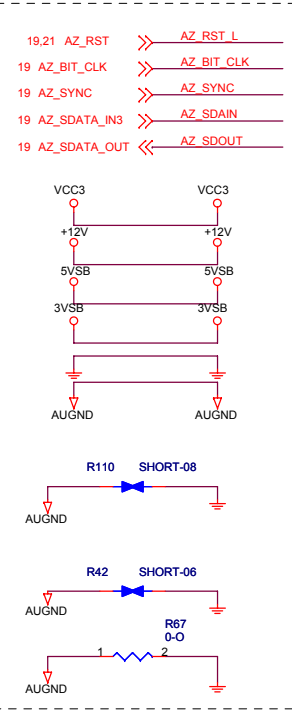
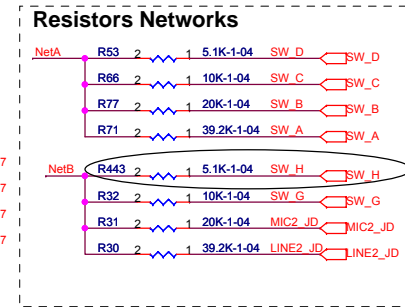


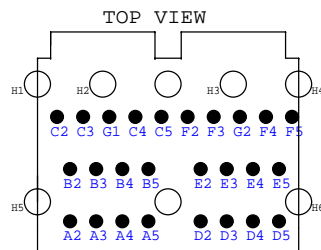
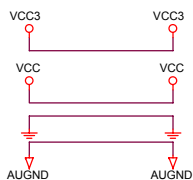
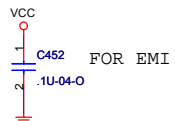
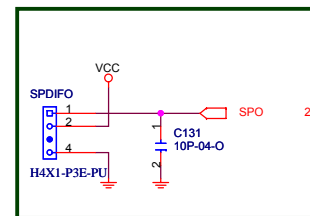
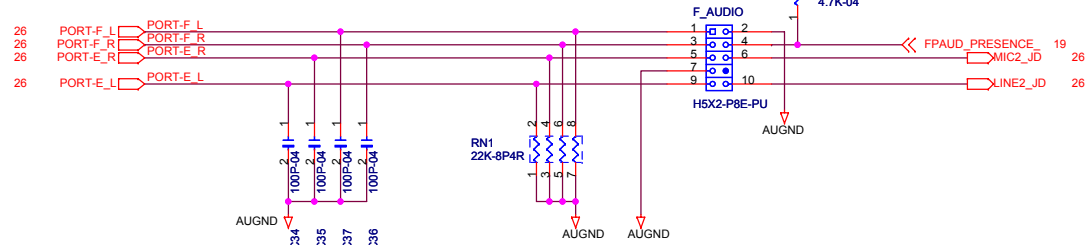
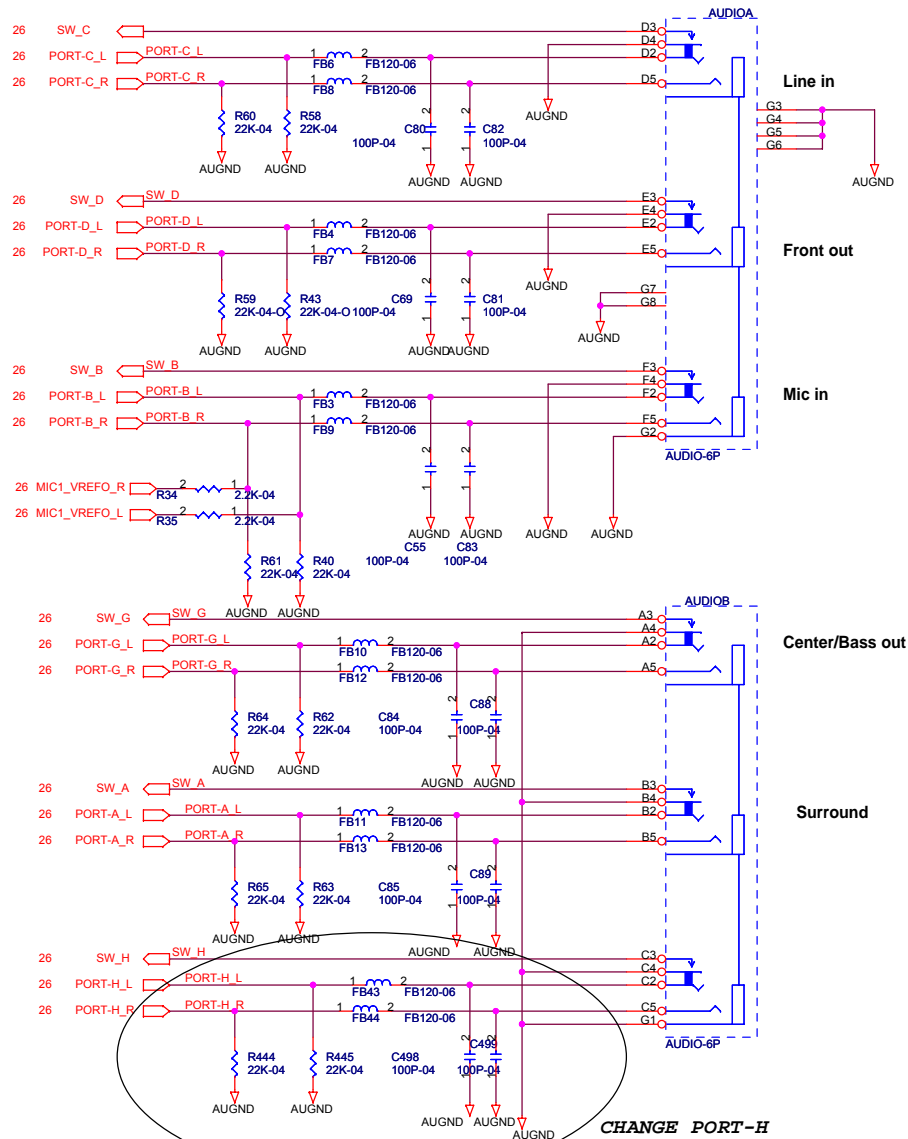
When you found some bug, please inform Ren(ext)1655 to update circuit.

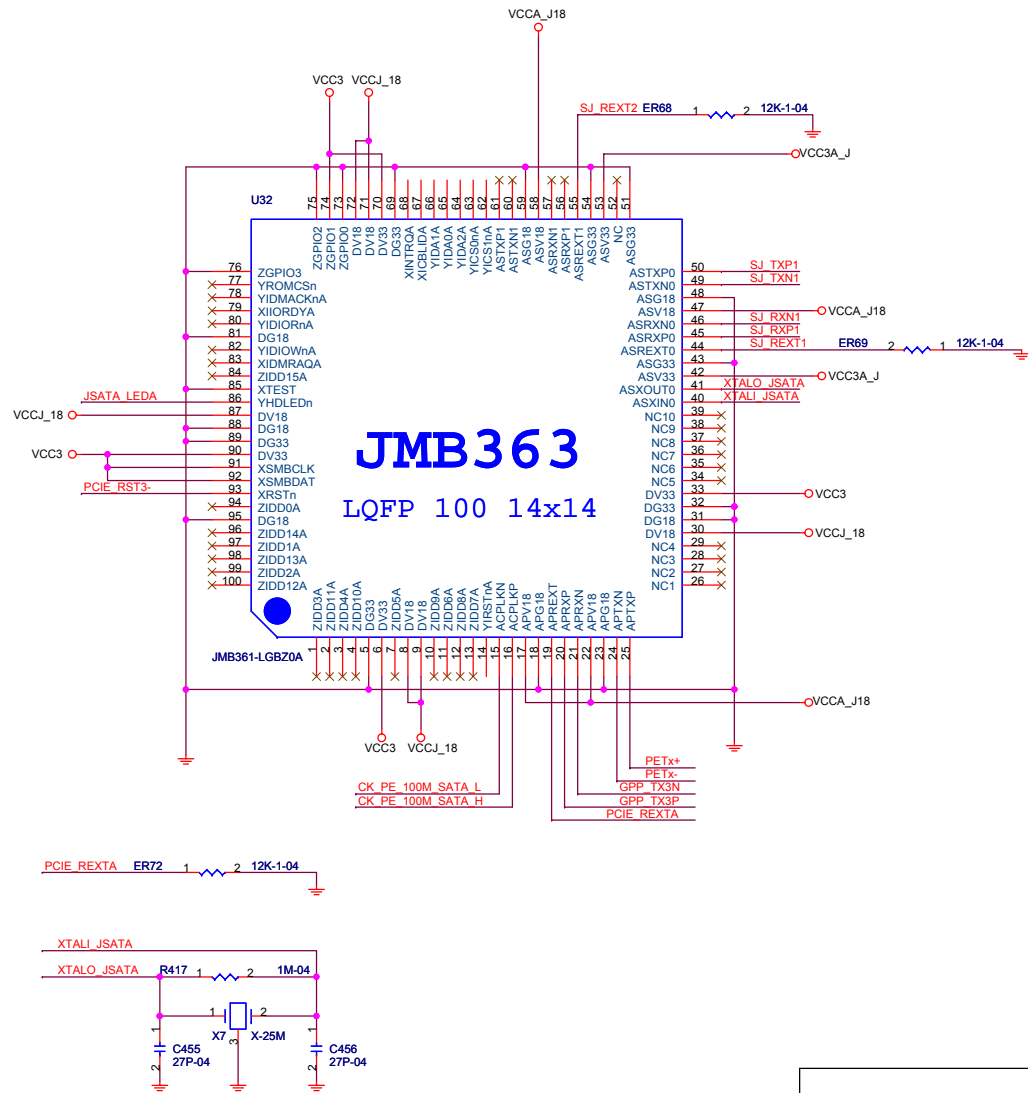
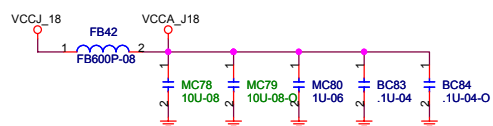
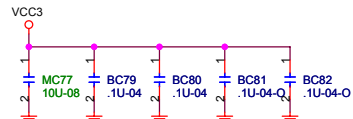
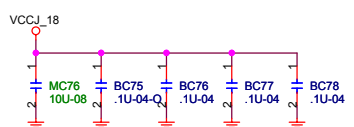
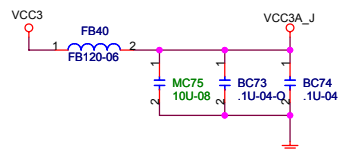
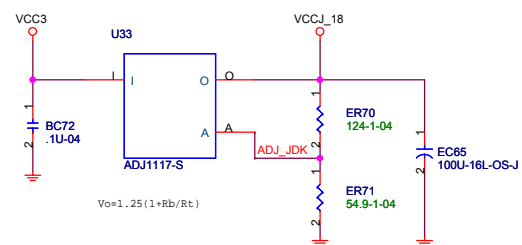
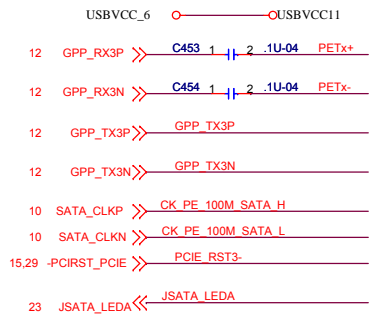
BOM Difference

Power Difference

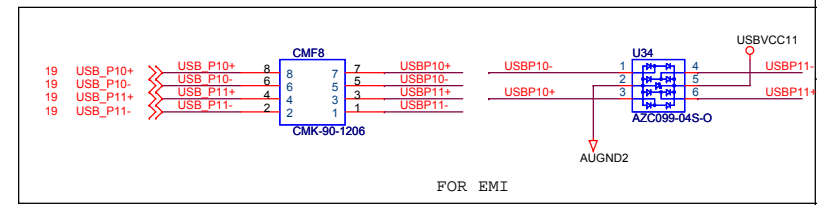
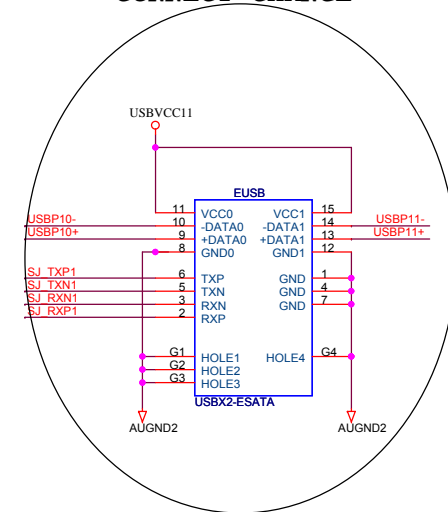
[illegible]

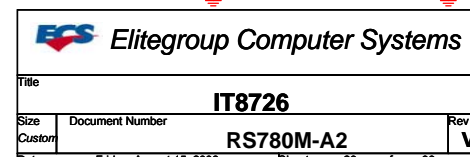


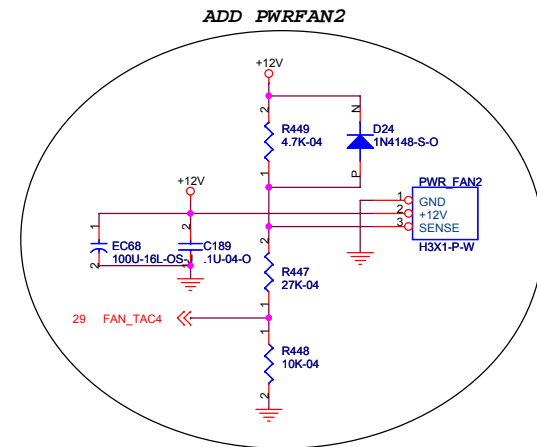
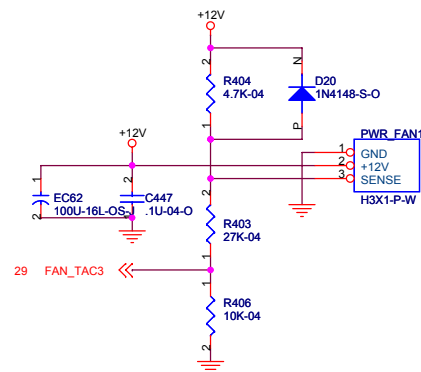
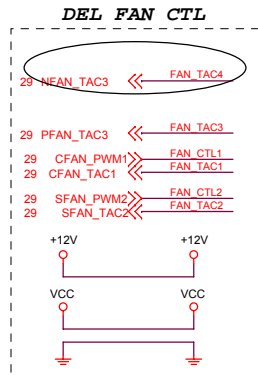
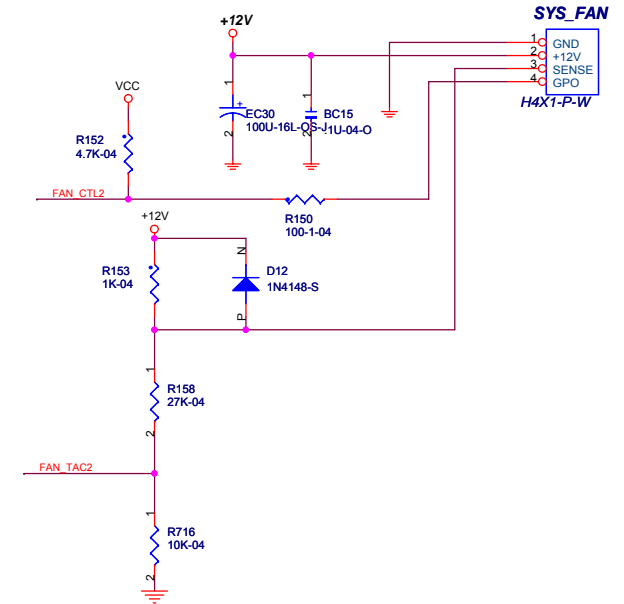
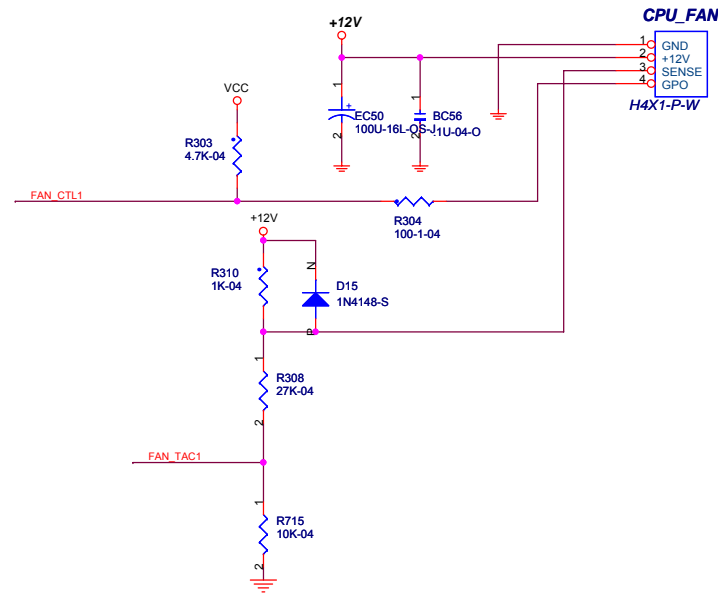


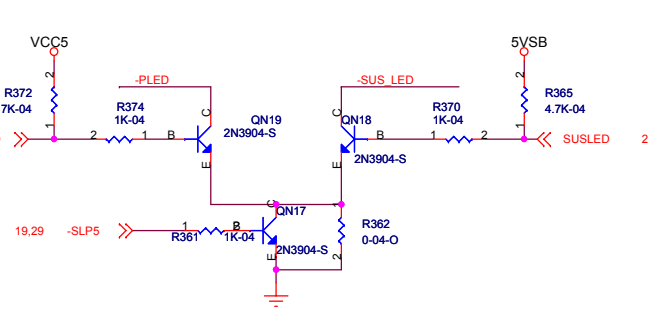
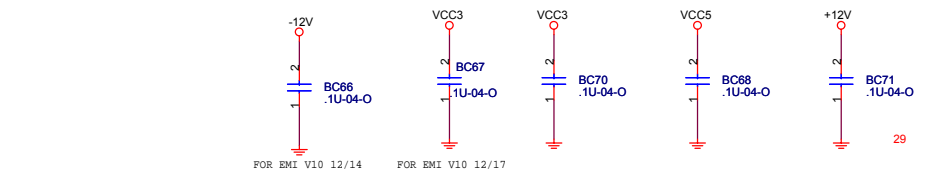
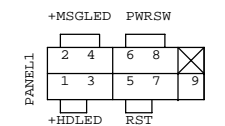
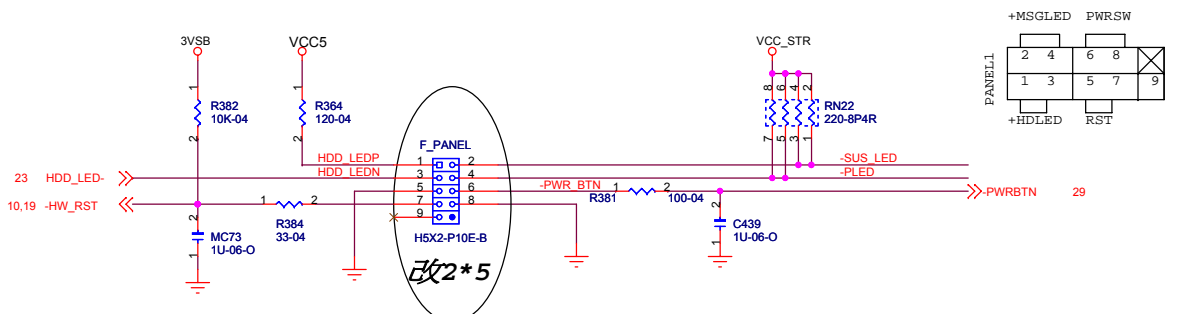
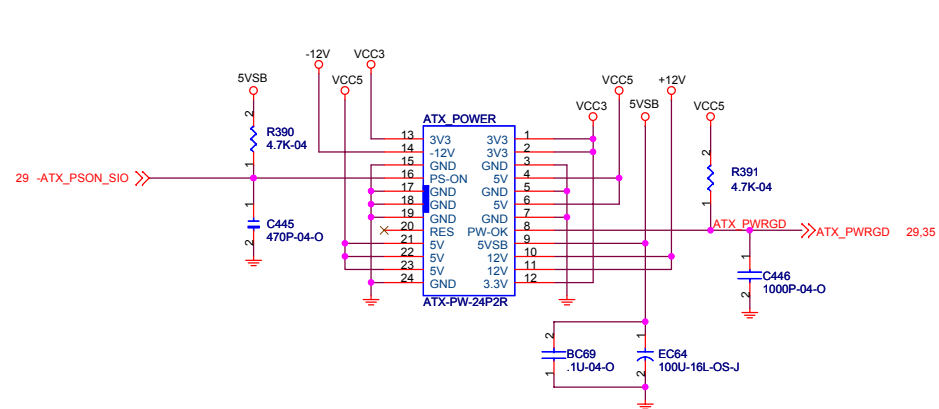


CONNECT CHANGE

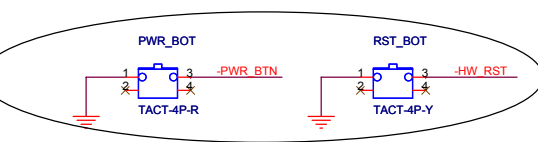
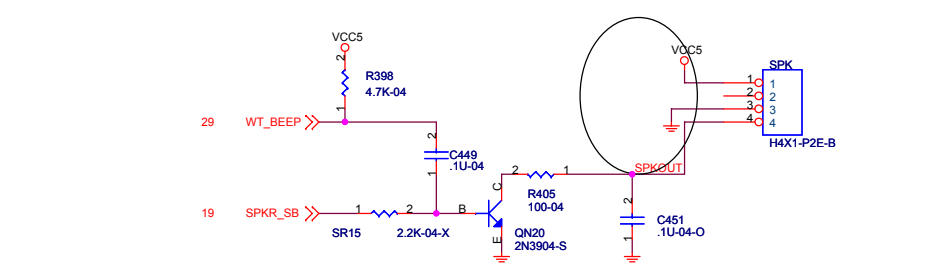


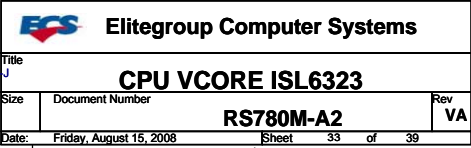




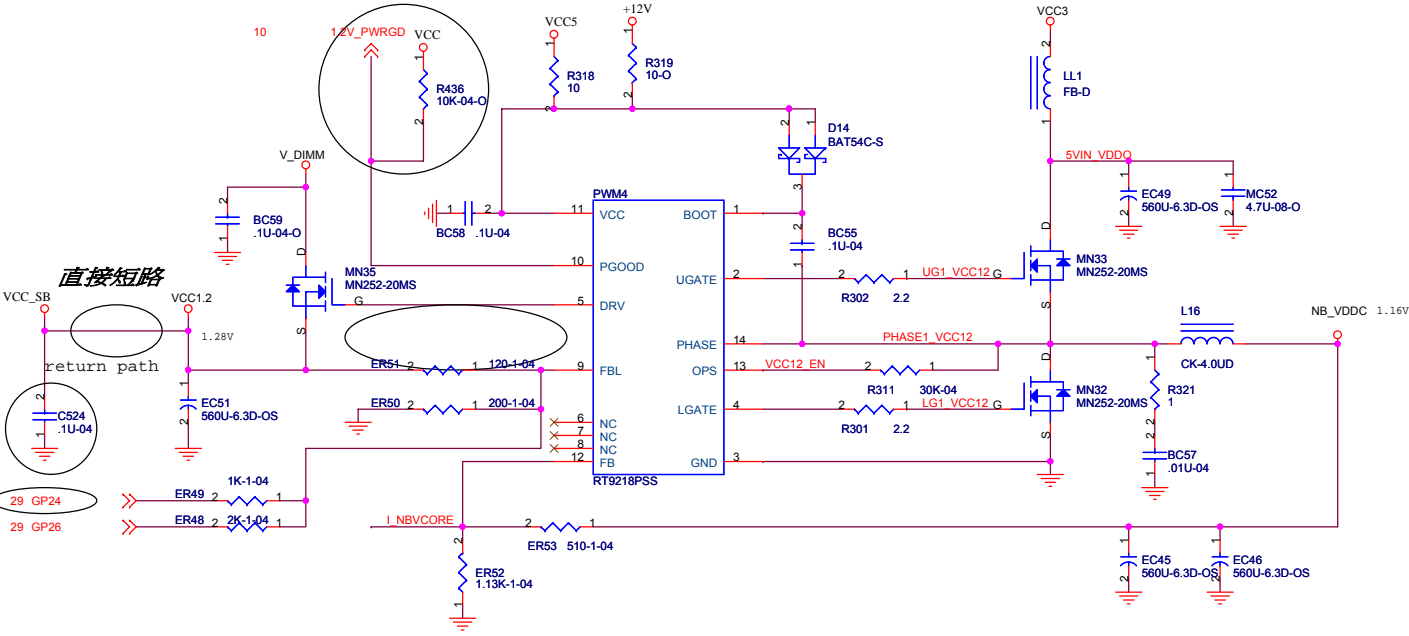


	AC_ON	S0	S1	S3	S5
SUSLED(GP41)	0	0	B	B	0
PLED(GP31)	0	1	1	0	0
-SUSLED(PIN2)	1	1	B	B	1
-PLED(PIN4)	1	0	0	1	1
LED STATE	OFF	Green	G-blink	Y-blink	OFF

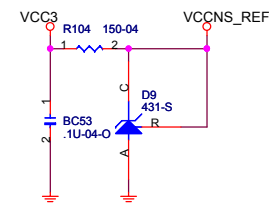
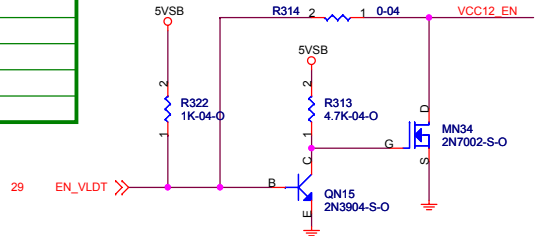




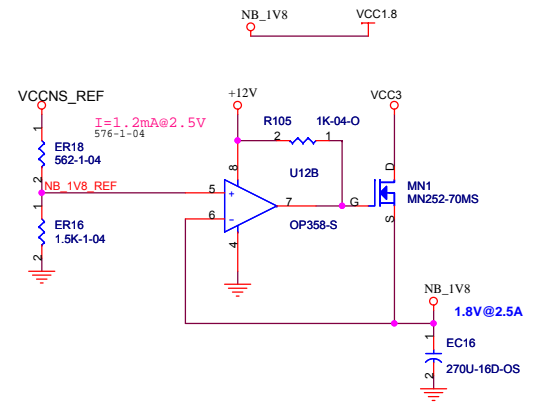
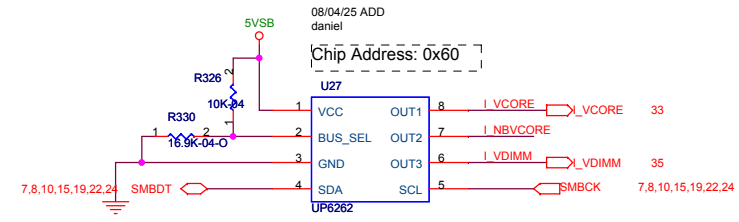
OD PULL HI



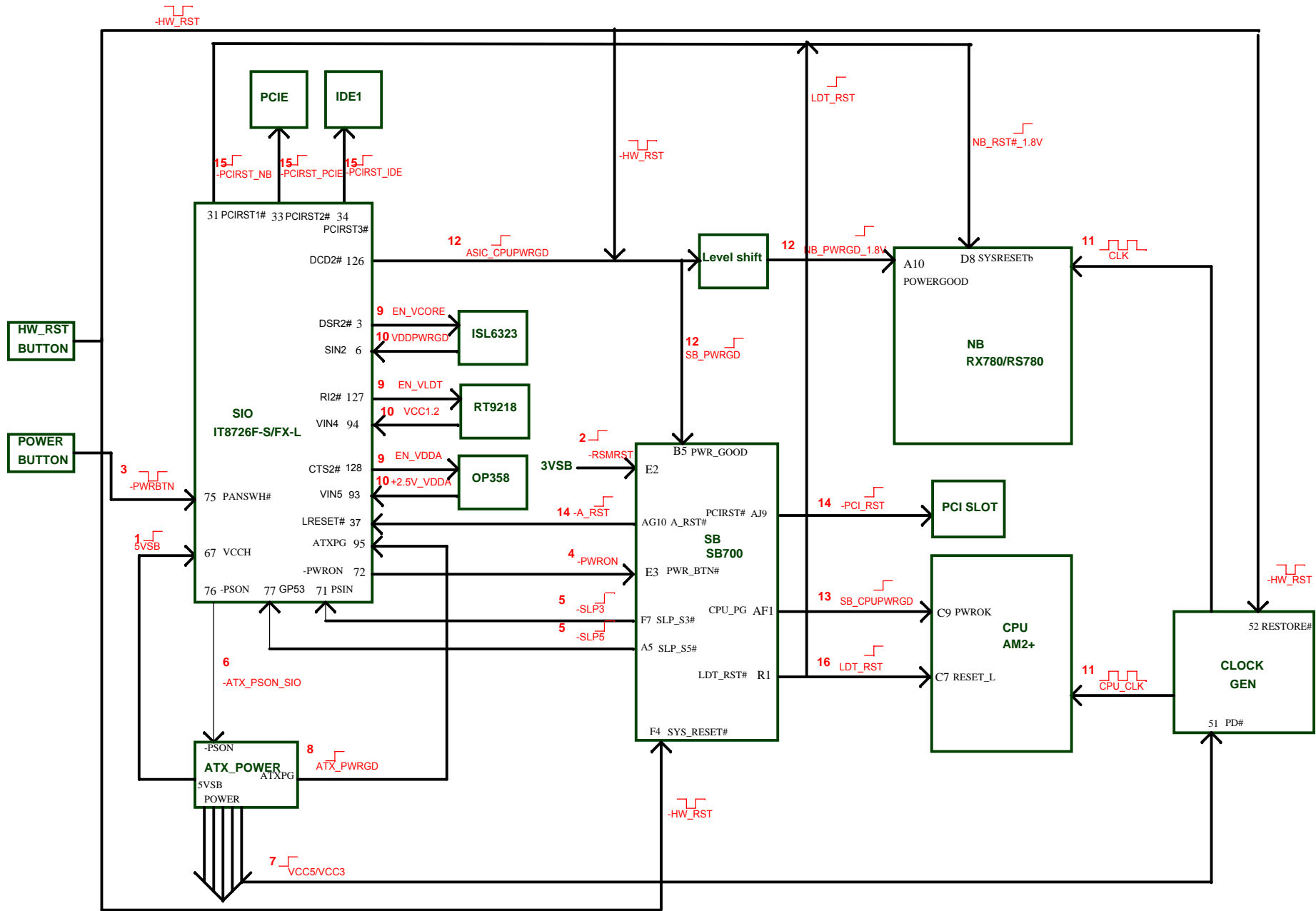
	GP24	GP26
1.35V	0	0
1.3V	0	1
1.25V	1	0
1.2V	1	1

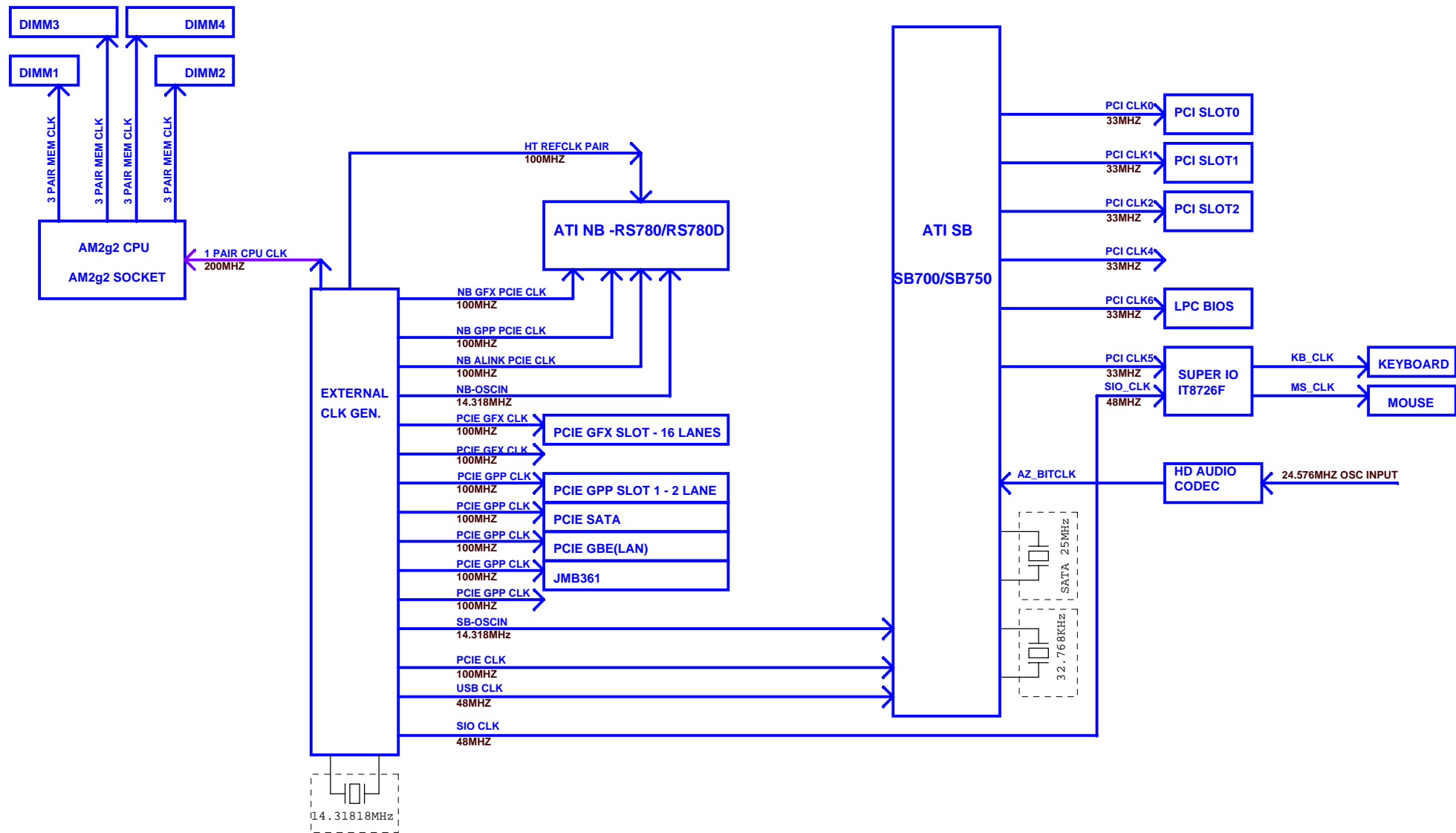


uP6262的電流輸出與ΔVout的關係如下:
選取從uP6262輸出的方向為正, 則VCORE, CPUVTT及V_DIMM的ΔVout為:
 $\Delta V_{out} = -I_c \cdot R_{FB}$
RFB為:
1. For VCORE, RFB = ER43 = 2K OHM;
2. For CPUVTT, RFB = ER52 = 931 OHM;
3. For V_DIMM, RFB = ER56 = 887 OHM.



Del SD






```
SB600 PinD23 GPIO5:audio PANEL_DETECT(1:no,0:yes)
SB600 PinC26 GPIO8:PCIEI GFX1_PRSNT-
SB600 PinD26 GPIO9:-P66DET
```

```
8726 GPIO使用:
Pin14-GPIO34用作WT_BEEP
Pin13-GPIO35 用作NB_PWM_enable控制
Pin18-GPIO31 PLED
Pin78-GP41 SUSLED
Pin28-GP17 -WP_ROM
Pin79-GPIO40: SIO_VDUAL control 5vdual
Pin28-GP22-THRM
Pin27-GP20:-LPC_SMI
Pin70-GP46:Control v_dimm
```

PCI SLOT1:REQ0;GNT0 IDSEL:21 INT:EFGH
PCI SLOT2:REQ1;GNT1 IDSEL:22 INT:FGHE
PCI SLOT3:REQ2;GNT2 IDSEL:23 INT:GHEF

```
NB_PWM1: Regulate VCC_CORE
NB_PWM2: Regulate V_DIMM
```

```
GPP:0-->PCIEx1
GPP:1-->PCIEx1
GPP:2-->GIGA LAN
```

For 103
X5(WIRE)



PCB Impedance control

Impedance (ohm)	Trace Width (mil) (S/W/S)	Trace Length (inch)	Pre-preg	
60	5 (20/5/20)	6	2116	v
50	4 (50/4/50)	6	1080	
42	6 (50/6/50)	6	1080	

1)Circuit type 1

Layer 1:TOP

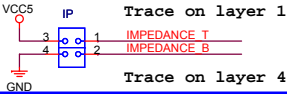
Layer 2:GND

Layer 3:LNNER

Layer 4:PWR

Layer 5:GND

Layer 6:BOTTOM



- Notes:
- 1). "PWR" net means inner power plane under impedance trace.
 - 2). "GND" net means inner ground plane under impedance trace.
 - 3). IP1 footprint is J2X2_IP
 - 4). After nelist running, please specially take care the single net name: "IMPEDANCE_T" and "IMPEDANCE_B".

